IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Hansen, et al. Application No.: 10/757,925 Filed: January 16, 2004 For: METHOD AND SOFTWARE FOR PARTITIONED GROUP ELEMENT SELECTION OPERATION	Examiner: Jesse R. Moll Technology Center/Art Unit: 2181 Confirmation No.: 5116

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF JOHN MOUSSOURIS UNDER 37 CFR § 1.131

Sir:

I, John Moussouris, hereby declare the following to be true:

BACKGROUND

1. I am a co-inventor of United States Patent Application No. 10/757,925 (the '925 application). I understand that this application is currently being examined by the patent office. Among other things, this declaration describes certain activities that occurred prior to August 1, 1995, through August 16, 1995, the filing date of U.S. Patent Application Serial number 08/516,036 (the '036 application). The '036 application matured into U.S. Patent number 5,742,840 (the '840 patent), which is the original parent of the '925 application. Attached to this declaration are various documents that evidence conception and diligence in reducing certain inventions claimed in the '925 application to practice.

2. Prior to founding MicroUnity, I co-founded (and served as vice president of research and development at) MIPS Computer Systems, Inc. ("MIPS"), where I staffed and managed the development of a RISC microprocessor and math coprocessor, two chips that led the industry in performance for several years.

3. Before co-founding MIPS, I was an IBM Visiting Scholar at Stanford University's Center for Integrated Systems. At IBM T.J. Watson Research Lab in Yorktown, I was a founding member of a VLSI research project that developed a microprocessor based on the 801 RISC architecture. I also received an Outstanding Innovation Award for design of run-length-limited coding hardware used in IBM disk products. Before IBM, I was a research staff member at the MIT Laboratory for Computer Science.

4. I received my A.B. degree in Physics from Harvard College and a masters degree in mathematics and doctoral degree in mathematical physics from Oxford University, where I was a Rhodes Scholar.

5. I founded MicroUnity in 1988. More specifically, prior to August 1, 1995, and through August 16, 1995, I was the CEO and Chairman of the Board of MicroUnity. As such, I have personal knowledge of MicroUnity's efforts toward implementing the Terpsichore system.

6. I am currently a shareholder in MicroUnity. I own approximately 69 percent of the shares of the company on a fully diluted basis. My current position at MicroUnity is CEO and Chairman of the Board.

7. All of the exhibits attached to this declaration are part of MicroUnity's records, and the exhibits are authentic and true copies of original documents (except for the redactions specified below and, in some cases, page numbers used for ease of reference).

CONCEPTION

8. Along with my co-inventor, Craig Hansen, I conceived of a METHOD AND SOFTWARE FOR PARTITIONED GROUP ELEMENT SELECTION OPERATION that included the following claims:

> 1. A method of processing data in a programmable processor, the method comprising: decoding a single instruction for selectively arranging data, specifying a data selection operand and a first and a second register each having a register width, the first and second registers providing a plurality of data elements each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields each independently selecting one of the plurality of data elements; and for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.
>
> 11. The method of claim 1 wherein for each field of the data selection operand, a relative location of the field within the data selection operand corresponds to a relative location of the predetermined position within the catenated result.
>
> 12. The method of claim 1 further comprising: decoding a second single instruction specifying a third and a fourth register each containing a plurality of floating-point operands; multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products; and providing the plurality of products to partitioned fields of a result register as a catenated result.
>
> 14. A computer-readable medium: having instructions that instruct a computer system to perform operations, at least some of the instructions including a group element selection instruction for selectively arranging data in a programmable processor, the group element selection instruction capable of instructing a computer to perform operations comprising: decoding the group element selection instruction specifying a data selection operand and a first and a second register each having a register width, the first and second registers providing a plurality of data elements each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields each independently selecting one of the plurality of data elements; and for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.

24. The computer-readable medium of claim 14 wherein for each field of the data selection operand, a relative location of the field within the data selection operand corresponds to a relative location of the predetermined position within the catenated result.

25. The computer-readable medium of claim 14 wherein at least some of the instructions further include a group floating point multiply instruction for multiplying floating point data in a programmable processor, the group floating point multiply instruction capable of instructing the computer to perform operations comprising: decoding the group floating point multiply instruction specifying a third and a fourth register each containing a plurality of floating-point operands; multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products; and providing the plurality of products to partitioned fields of a result register as a catenated result.

9. It is my understanding that the claims recited above have been rejected in the outstanding office action based on a patent issued to Ruby Lee and assigned to Hewlett Packard.

10. The conception (before the date of the Ruby Lee patent) of the above-recited claims of the METHOD AND SOFTWARE FOR PARTITIONED GROUP ELEMENT SELECTION OPERATION is shown, in part, in Exhibits 1-2, attached hereto. Certain dates of Exhibits 1-2 showing conception have been redacted in accordance with standard practice and indicated with the phrase "REDACTED". Notwithstanding these redactions in Exhibits 1-2, all of the redacted dates are prior to August 1, 1995.

Exhibits 1 and 2 – Presentation to Cray Research, Inc. and the pre-filing version of the Terpsichore System Architecture Manual

11. Exhibit 1 is a presentation made to Cray Research, Inc. pursuant to a confidentiality agreement between MicroUnity and Cray Research, Inc., with dates redacted. The presentation is a technology overview of the Terpsichore System

Architecture and further describes certain subject matter disclosed and claimed in the '925 application.

12. Exhibit 2 is a version of the Terpsichore System Architecture manual that Mr. Hansen authored prior to August 1, 1995, with the dates redacted. The manual describes certain subject matter disclosed and claimed in the '925 application. This manual was updated while work on the Terpsichore system progressed. A later version of this manual, dated August 2, 1995, was filed as an appendix in the '036 application.

13. Exhibits 1 and 2 are described in detail in Mr. Hansen's declaration filed concurrently herewith. In particular, I refer the PTO to paragraphs 9 – 15 of Mr. Hansen's declaration.

14. Exhibits 1 and 2 were prepared prior to August 1, 1995, prior to which I spent a considerable amount of time conceiving and developing the Terpsichore System in conjunction with Mr. Hansen. As indicated by accompanying Exhibits, Mr. Hansen and I conceived the fundamental features of the Terpsichore System prior to Augustl 1, 1995, which we believed would work for their intended purpose once sufficient prototyping and testing efforts were performed.

DILIGENCE

15. From just prior to August 1, 1995 through August 16, 1995, I and others at MicroUnity, as well as MU's legal patent prosecution team, were diligent in our efforts to perform detailed design, to build and to test the Terpsichore system and to file the '036 application, which matured into the '840 patent, which is the original parent of the '925 application. MicroUnity's efforts to further design, build and test the Terpsichore system included the incorporation of features conceived prior to August 1, 1995 into integrated

circuitry implementing the Terpsichore system and the development work associated with such incorporation.

16. The evidence showing diligence includes: attorney billing records from MicroUnity's patent prosecution team; modifications made to the electronic databases used to manufacture integrated circuits implementing the Terpsichore system; email communications among the MicroUnity design team making modifications to the electronic databases; and MU payroll records showing salary payments to team members.

Exhibit 3 – Attorney Billing Records

17. Exhibit 3 is an invoice from the law firm of Willian, Brinks, Hofer, Gilson & Lione, MicroUnity's patent prosecution counsel. These documents are explained in detail in paragraph 18 of Mr. Hansen's declaration filed concurrently herewith, and I refer the PTO to that paragraph of Mr. Hansen's declaration.

Exhibits 4A-4D – Logs of Modifications to the Electronic Databases

18. MicroUnity's Terpsichore system was intended to be implemented in integrated circuit form. *See, e.g.*, Exhibit 1 at pages MU0020321-356 (discussing the status of MicroUnity's integrated circuit fabrication facility). From a time prior to August 1, 1995, through August 16, 1995, the individuals on the MU design team spent a substantial amount of their time in building elaborate databases (sometimes called "tape outs" or "physical layouts") for the Terpsichore system. Exhibits 4A-4D represent weekly logs of modifications to the electronic databases for the Terpsichore system from just prior to August 1, 1995, through August 16, 1995. These documents are explained in detail in paragraphs 19 - 23 of Mr. Hansen's declaration filed concurrently herewith, and I refer the PTO to those paragraphs of Mr. Hansen's declaration.

Exhibits 5 – Emails among the MicroUnity Design Team

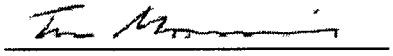
19. Further evidence of MicroUnity's efforts to implement the Terpsichore system in integrated circuit form is shown in email communications among the members of MicroUnity's design team from the time just prior to August 1, 1995, through August 16, 1995. These emails are grouped and attached hereto as Exhibits 5. These emails are explained in detail in paragraphs 24-25 of Mr. Hansen's declaration filed concurrently herewith, and I refer the PTO to those paragraphs of Mr. Hansen's declaration.

Exhibit 6 – Payroll Records

20. Exhibit 6 reflects various MicroUnity payroll records from just prior to August 1, 2005 through August 16, 1995. These documents show that MicroUnity spent approximately $138,000 to $139,000 per pay period from just prior to August 1, 1995 through August 16, 1995 to develop the Terpsichore system. These documents are explained in detail in paragraph 26 of Mr. Hansen's declaration filed concurrently herewith, and I refer the PTO to that paragraph of Mr. Hansen's declaration.

21. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and the these statements are made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, and any patent issuing thereon, or any patent to which this declaration is directed.

January 7, 2009
Date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